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for ASIC and FPGA - Mercora Technologies IP Cores has announced shipments of an FPGA version of the MACsec statistics add-on core for its popular MSP10 MACsec encryption/decryption core for line-speed MACsec processing targeting the 100 Gbps Page 8/25

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intoPIX - PR -JPEG2000 IP cores on Altera FPGA Devices  
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## Floating-Point IP Cores User Guide

The SHA256 IP core is a high performance implementation of the SHA-256 Message Digest algorithm, a one-way hash function, compliant with FIPS 180-2. The core is composed of two main units, the SHA256 Engine and the Padding Unit as shown in the block diagram. The SHA256 Engine applies the SHA256 loops on a single 512-bit message block, while the Padding Unit splits the input message into 512-bit blocks and performs the message padding on the last block of the message.

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SHA-256 IP Core Secure Hash Function - Alma Technologies  
Altera AES IP Cores perform data encryption and/or decryption as specified by the Federal Information Processing Standard (FIPS) 197, Advanced Encryption Standard (AES).

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2.1. Installing and Licensing Intel FPGA IP Cores. The Intel Quartus Prime software installation includes the Intel FPGA IP library. This library provides many useful IP cores for your production use without the need for an additional license.

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Some Intel FPGA IP cores require purchase of a separate license for production use.

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